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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,332	12/31/2003	Bernhard Kowalski	INF-125	8131

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,332	KOWALSKI ET AL.	
	Examiner	Art Unit	
	Matthew E Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18 and 19* is/are allowed.

6)☒ Claim(s) *1,2,6 and 9* is/are rejected.

7)☒ Claim(s) *3-5,7,8 and 10-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Prior Art Figures 1 and 2 (APAF) in view of Wang (US 6,617,180 B1).

In re claim 1, the APAF 1 and 2 show an integrated circuit comprising a vertical FET access transistor array formed into the depth of a substrate (10) in active webs

which run parallel in the lateral direction of the integrated circuit and are implemented as vertical trenches [0016-0018]; an array of storage capacitors (6, 9), wherein each storage capacitor is associated with a vertical FET access transistor and is formed in a deep trench on a face of a section of an active web which forms the vertical FET access transistor; and a series of wordlines [0018] arranged along the active webs. The APAF does not show a series of bitlines intersecting the wordlines and the process diagnoses test structure. Although bitlines formed in a memory array are well known in the art and the APAF neglects to mention them, Wang shows (fig. 9) a series of bitlines (65) intersecting the wordlines (63) of memory array. Capacitors and transfer FETS of the device are formed below the wordlines and bitlines. Wang also includes an array process diagnosis test structure (45) (col. 9, lines 1-9 discloses structures 45 and 47 for testing during the manufacturing process of the DRAM), wherein the process diagnosis test structure (connected to pad 1) is connected to the wordlines and wherein the connection to the wordlines forms a wordline comb structure. With this structure, it can be determined if there defects or problems with the memory device (col. 5, lines 19-34). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the wordlines of the APAF by providing a comb structure to the wordlines as taught by Wang to determine if there are defects or bridging problems within the memory array.

In re claim 2, Wang shows (fig. 9) the process diagnosis test structure is connected to the bitlines (pads 2 in test region 45) and wherein the connection to the bitlines forms a bitline comb structure (at the end of bitlines 65).

In re claim 6 and 9, Wang shows (fig. 9) that the bitline comb structure comprises a first bitline comb (at pad 2) connected to a first series of non-adjacent bitlines (65 with bitlines 67 between them) along a third edge of the transistor array, wherein the spacing between each successive bitline in the first series of non-adjacent bitlines is defined by a parameter m; a second bitline comb (at pad 4) connected to a second series of non-adjacent bitlines (67 with bitlines 65 between them) along a fourth edge of the transistor array opposite to the third edge, wherein the spacing between each successive bitline in the fourth series of non-adjacent bitlines is defined by the parameter m, and wherein the first series and second series of bitlines are offset to include no common bitlines. The value of m is equal to 1 and not 2, however, It would have been obvious to one of ordinary skill in the art to use three, four, etc., spacings of bitlines since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).* See also MPEP 2144.04 VI. (B).

Allowable Subject Matter

Claims 3-5, 7, 8, and 10-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 18 and 19 are allowed.

The following is an examiner's statement of reasons for allowance: as recited in claim 18, the prior art references, alone or in combination, do not show an integrated circuit for testing performance of memory devices comprising an array of memory cells wherein each cell includes a vertical FET access transistor and a deep trench capacitor associated with the access transistor, and a test structure comprising a plurality of comb-like structures, wherein each of a first pair of comb-like structures link a series of regularly spaced non-adjacent wordlines together, wherein the pair of comb-like structures connect to wordlines of the array at opposite edges, and wherein the comb-like structures are mutually offset such that no wordlines are shared between the two comb-like structures.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Saitoh et al. (US 5,844,915), Churchill et al. (US 6,388,927 B1) and Weiner et al. (US 2003/0003611 A1) also show test methods including comb-like structures in a memory array.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is

(571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
November 2, 2004

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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